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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/797,754	03/09/2004	Kyu-Charn Park	4591-369	4232

7590 05/18/2005

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EXAMINER	
DICKEY, THOMAS L	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 05/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/797,754	PARK ET AL.	
	Examiner	Art Unit	
	Thomas L. Dickey	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *12-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7-10 and 20* is/are rejected.

7)☒ Claim(s) *2,6 and 11* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/9/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restriction

1. Applicant's election without traverse of Group II, claims 1-5, in the Paper filed 03/28/2005 is acknowledged.

Oath/Declaration

2. The oath/declaration filed on March 9, 2004 is acceptable.

Drawings

3. The formal drawings filed on March 9, 2004 are acceptable.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

5. The Information Disclosure Statement filed on March 9, 2004 has been considered.

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1,3-5,7-10 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by PIO ET AL. (5,894,146).

With regard to claims 1, 3, and 4 Pio et al. discloses a non-volatile memory element with a memory gate pattern 2 and a selection gate pattern 3 separated from each other and arranged on a semiconductor substrate (note column 4 line 23), the memory gate pattern 2 comprising a tunnel dielectric layer 4, a floating gate 6, a first inter-gate dielectric 7 (the right-hand element 7 in figure 8), a control gate electrode 10, and a control gate mask conductive layer 9 formed on the first and second inter-gate dielectrics 7; which are sequentially stacked, the selection gate pattern 3 comprising a gate dielectric layer 12, a bottom gate pattern 5, a second inter-gate dielectric 7 (the left-hand element 7 in figure 8), a top gate pattern 8 (the left-hand 8 in figure 8) electrically connected to the bottom gate

pattern 5, which are sequentially stacked, and a top gate mask conductive layer 9 formed on the first and second inter-gate dielectrics 7; wherein the width of the second inter-gate dielectric 7 (note figure 1 and column 5 lines 24-28, showing removal of dielectric material in region c2, narrowing the second inter-gate dielectric) is narrower than the width of the bottom gate pattern 5. Note figures 1-8 and column 5 lines 15-28 of Pio et al.

With regard to claims 5 and 6-10 Pio et al. discloses a non-volatile memory element with a device isolation layer 20 disposed on a semiconductor substrate (note column 4 line 23) to define a plurality of active regions 14-15-16; selection lines 5-12 extending across the active regions 14-15-16, the selection lines 5-12 each including a bottom gate pattern 5, a second inter-gate dielectric 7 (the left-hand element 7 in figure 8) including at least a single dielectric layer of SiN, which has a dielectric constant higher than that of silicon oxide, crossing over the active regions 14-15-16, and a top gate pattern 8 (the left-hand 8 in figure 8), which are sequentially stacked; a top gate mask conductive layer 9 formed on the first and second inter-gate dielectrics 7; and a plurality of word lines 10 disposed between the selection lines 5-12 to extend across the active regions 14-15-16 and including a floating gate 6 pattern interposed between each of the active regions 14-15-16 and one of the word lines 10, wherein the bottom gate pattern 5 disposed under the top gate pattern 8-9 to extend across the active regions 14-15-16, a first inter-gate dielectric 7 (the right-hand element 7 in figure 8) including at least a single dielectric layer of SiN, which

has a dielectric constant higher than that of silicon oxide, a control gate electrode 10, and a control gate mask conductive layer 9 formed on the first and second inter-gate dielectrics 7; which are sequentially stacked, wherein the width of the second inter-gate dielectric 7 (note figure 1 and column 5 lines 24-28, showing removal of dielectric material in region c2, narrowing the second inter-gate dielectric) is narrower than the width of each selection line 5-7. Note figures 1-10 and column 5 lines 15-28 of Pio et al.

With regard to claim 20 Pio et al. discloses a non-volatile memory element with a semiconductor substrate (note column 4 line 23); a gate line 5-12 formed on the substrate, the gate line 5-12 including a gate dielectric layer 12, a bottom gate pattern 5, an inter-gate dielectric 7and a top gate pattern 8 (the left-hand 8 in figure 8), which are sequentially stacked on the substrate, wherein the width of the inter-gate dielectric is narrower than the width of the bottom gate pattern 5. Note figures 1-8 and column 5 lines 15-28 of Pio et al.

Allowable Subject Matter

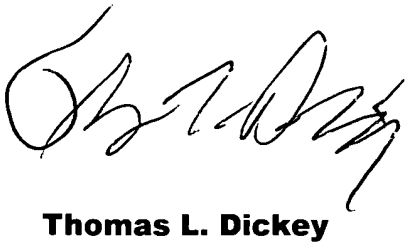
8. Claims 2,6, and 11 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thomas L Dickey whose telephone number is 571-272-1913. The examiner can normally be reached on Monday-Thursday 8-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan J Flynn can be reached on 571-272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Thomas L. Dickey
Patent Examiner
Art Unit 2826
05/05